for each gate region, a dielectric carrier separation layer formed at the periphery of said gate region.

8. The method of claim **7**, wherein the source region has width d that is greater than $2W_{D0}$, wherein W_{D0} equals the depletion layer thickness of the SIT at $V_{GS}=0$.

9. The method of claim **7**, wherein the semiconductor material comprises silicon and the dielectric carrier separation layer comprises silicon oxide.

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